REMARKS

Upon entry of the foregoing amendment, claims 1, 3-6 and 8-10 are pending in the application with claims 1 and 6 being the independent claims. Claims 2, 7 and 11-12 are canceled without prejudice to or disclaimer of the subject matter therein. These changes introduce no new matter and their entry is respectfully requested.

Double Patenting

Claims 1 and 4 are rejected under the doctrine of obviousness-type double patenting as being unpatentable over U.S. Patent No. 6,959,052 to Harada et al. ("Harada '052") in view of U.S. Patent No. 6,169,751 to Shirakata ("Shirakata"). The Examiner states that Harada '052 "fails to teach a delay unit, said delay unit outputs a delay signal which is obtained by delaying the reception signal by a predetermined delay time wherein the predetermined delay time is equal to or smaller than a time required for processes by said replica unit and said estimation unit." The Examiner relies upon Shirakata to overcome the shortcoming in the teachings of Harada '052. Namely, the Examiner asserts that Shirakata teaches providing a plurality of delayers that delay a signal by a predetermined time that is not greater than one cycle of a clock signal.

Claim 1, as amended, recites a receiving device that includes a delay unit that outputs a delay signal that is obtained by delaying a reception signal by a predetermined delay time. The claim further recites that the predetermined delay time is longer than a symbol time length of the reception signal and is equal to a time required for processes by a replica unit and an estimation unit, in order for an equalizer/demodulator to compensate for each symbol of the reception signal with a transmission path characteristic which is estimated, by the estimation unit, for the symbol to be compensated for by the equalizer/demodulator.

Shirakata teaches providing a plurality of delayers which delay a signal by a predetermined time where the range is not greater than one cycle of a clock signal. Here, in orthogonal frequency division multiplex ("OFDM") based communications, generally, the time length for one OFDM symbol is equal to or greater than one cycle of a clock time. For instance, in one implementation example made by the Applicants, the time length of one symbol is equal to 80 clock cycles.

However, if the transmission path characteristic changes in this process performance time, it presents a problem. In particular, the difference between the estimated transmission path characteristic and the actual transmission path characteristic is large, thereby causing deterioration in the receiving characteristic.

Therefore, the time required for processes by the replica unit and the estimation unit of the present invention is longer than one symbol time length, i.e., one cycle of a clock time. Typically, the time length of thus occurring delay corresponds to a few tens of cycles of clock time.

As discussed above, the delayer of Shirakata delays a timing signal by one clock time, which is shorter than the symbol time length. Therefore, the combination of Harada '052 and Shirakata fails to disclose the features recited in claim 1.

Furthermore, in the present invention, the replica unit, in processing a given received symbol, uses a path obtained for those symbols processed prior to the received symbol, performs compensation and generates a replica symbol.

On the other hand, the equalizer/demodulator of the present invention performs compensation by use of a path characteristic obtained at a time at which the received symbol is received, and obtains a transmission symbol.

Therefore, it follows that the path characteristics used in one of two compensations are off by one with respect to the path characteristics used in another compensation. As a result, such a configuration is not disclosed in the combined references.

Additionally, the structure disclosed in Harada '052 is different from the present invention. In particular, the structure of Harada '052 uses a path characteristic obtained immediately before the reception of the received symbol, for performing the compensation of the same, to obtain a transmission symbol.

Harada '052 and Shirakata either alone or in combination fail to disclose or suggest the features recited in claim 1. Therefore, claim 1 is patentable over Harada '052 in view of Shirakata. Claim 4 depends from and includes all of the features of claim 1 and for at least the same reasons is patentable over Harada '052 in view of Shirakata.

Rejections under 35 U.S.C. § 101

Claims 11-12 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. Claims 11-12 have been canceled, rendering this rejection moot.

Rejections under 35 U.S.C. § 103

Claims 1-3, 6-8, and 11-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' description of the related art ("Background") in view of Shirakata. Similar to the double patenting rejection described above, the Examiner relies upon Shirakata for a teaching of a plurality of delayers that delay a signal by a predetermined time that is not greater than one cycle of a clock signal.

As described above, also with respect to the double patenting rejection, claim 1 recites a predetermined delay time that is longer than a symbol time length of a reception signal and is

equal to a time required for processes by a replica unit and an estimation unit. Similarly, claim 6, as amended, recites a receiving method that includes a predetermined delay time that is longer than a symbol time length of a reception signal and is equal to a time required for processes in a replica step and an estimation step.

Shirakata teaches providing a plurality of delayers which delay a signal by a predetermined time where the range is not greater than one cycle of a clock signal. The time required for processes by the replica unit and the estimation unit, and in a replica step and an estimation step, of the present invention, and as recited in the claims, is longer than one symbol time length, i.e., one cycle of a clock time.

Therefore, claims 1 and 6 are patentable over the Background in view of Shirakata. Claim 3 depends from and includes all of the features of claim 1 and for at least the same reasons is patentable over the Background in view of Shirakata. Claim 8 depends from and includes all of the features of claim 6 and for at least the same reasons is patentable over the Background in view of Shirakata. Claims 2, 7, 11 and 12 are canceled.

Claims 4 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Background in view of Shirakata and further in view of U.S. Patent Application Publication No. 2002/0126774 to Harada et al. ("Harada '774").

The Office Action states that claims 4 and 9 are rejected over the Background "and Shirakata (US20020141495) as applied to claims 1 and 6 above." However, U.S. Patent App. Pub. No. 2002/0141495 does not list Shirakata as an inventor, instead Hatamian is the only listed inventor on the publication, and that publication was not cited in the rejection of claims 1 and 6. Further, the text of the rejection refers to Shirakata in multiple instances. Therefore, for the

purpose of providing a complete response, Applicants assume the Examiner intended to cite U.S. Patent No. 6,169,751 to Shirakata.

As described above, both the Background and Shirakata fail to disclose a delay unit or a delay step wherein a signal is delayed by a predetermined time where the range is greater than one cycle of a clock signal. Harada '774 also fails to disclose such a feature. Claim 4 depends from and includes all of the features of claim 1. Therefore claim 4 is patentable over the Background in view of Shirakata and further in view of Harada '774. Claim 9 depends from and includes all of the features of claim 6. Therefore, claim 9 is patentable over the Background in view of Shirakata and further in view of Harada '774.

Claims 5 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' description of the related art and Hatamian as applied to claims 1 and 6 above, and further in view of U.S. Patent App. Pub. No. 2003/0108123 to Kroeger ("Kroeger"). Similar to the rejection of claims 4 and 9, the Examiner cited a publication number that does not list Shirakata as an inventor. For the other reasons described above, Applicants assume the Examiner intended to cite U.S. Patent No. 6,169,751 to Shirakata in order to provide a complete response.

Both the Background and Shirakata fail to disclose a delay unit or a delay step wherein a signal is delayed by a predetermined time where the range is greater than one cycle of a clock signal. Kroeger also fails to disclose such a feature. Claim 5 depends from and includes all of the features of claim 1. Therefore claim 5 is patentable over the Background in view of Shirakata and further in view of Kroeger. Claim 10 depends from and includes all of the features of claim 6. Therefore, claim 10 is patentable over the Background in view of Shirakata and further in view of Kroeger.

Conclusion

For at least the above reasons, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections. Applicants believe that a full and complete reply has been made to the outstanding Office Action and solicit allowance of the present application. If necessary, the Commissioner is authorized in this and concurrent replies to charge payment (or credit any overpayment) to Deposit Account No. 50-2298 in the name of Luce, Forward, Hamilton & Scripps LLP, for any additional fees required under 37 CFR 1.16 or 1.17.

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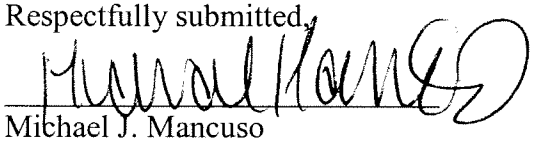
Respectfully submitted,



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